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**DOCUMENT-IDENTIFIER:   US 6460120 B1**

**TITLE:                Network processor, memory organization and  
methods**

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**US-CL-CURRENT:    711/148, 709/250 , 710/240 , 711/105 , 711/154 ,  
711/168  
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**US Patent No. - PN (1):  
6460120**

**Detailed Description Text - DETX (51):**

**A Control Point (CP) includes a System Processor that is  
connected to each  
of the configuration. The system processor at the CP, among  
other things,  
provides initialization and configuration services to the chip. The  
CP may be  
located in any of three locations: in the interface device chip; on**

the blade  
on which the chip is mounted or external to the blade. If external  
to the  
blade, the CP may be remote; that is, housed elsewhere and  
communicating by the  
network to which the interface device and CP are attached. The  
elements of a  
CP are shown in FIG. 17 and include memory elements (cache,  
flash and SDRAM), a  
memory controller, a PCI bus, and connectors for a backplane and  
for L1 network  
media.

**Detailed Description Text - DETX (60):**

One Interface device in the system is connected to the system processor via  
one of up to ten 10/100 Mbps Fast Ethernet ports or a single 1000  
Mbps Ethernet  
port. The Ethernet configuration to the system processor is  
placed in an  
EEPROM attached to the Interface device and loaded during  
initialization. The  
system processor communicates with all Interface devices in a  
system (see FIG.  
2), by building special Guided Frames encapsulated, for example,  
as ethernet  
frames or other media interfaces. The encapsulated Guided  
Frames are forwarded  
across the DASL link to other devices allowing all of the Interface  
devices in  
the system to be controlled from a single point.

**Claims Text - CLTX (8):**

**8. Apparatus comprising: a memory system including SRAM**

**modules and DRAM modules; said DRAM modules being responsive to a configuration signal that places said DRAM modules in a first mode of operation in which multiple consecutive Read or Write operations can be executed on banks within said DRAMs in a single access cycle or in a second mode of operation in which Read, and Write operations can be executed on selected banks within said DRAMs within an access cycle; a plurality of processors programmed to generate, among other things, the configuration signal, memory request signals and perform other tasks; and a network operatively coupling the plurality of processors to the memory system so that each processor in the plurality of processors has access to the SRAM modules and DRAM modules in said memory system.**